

**Tujuan:** Mampu menjelaskan teknologi dan struktur memory

**Pokok bahasan:** Memory Associative

**Reference:** Buku 1 ( Chapter 5.4 )

**Tugas:** None

**ASSOCIATIVE MEMORY**

ASSOCIATIVE-MEMORY (AM) VS. RANDOM-ACCESS-MEMORY (RAM)

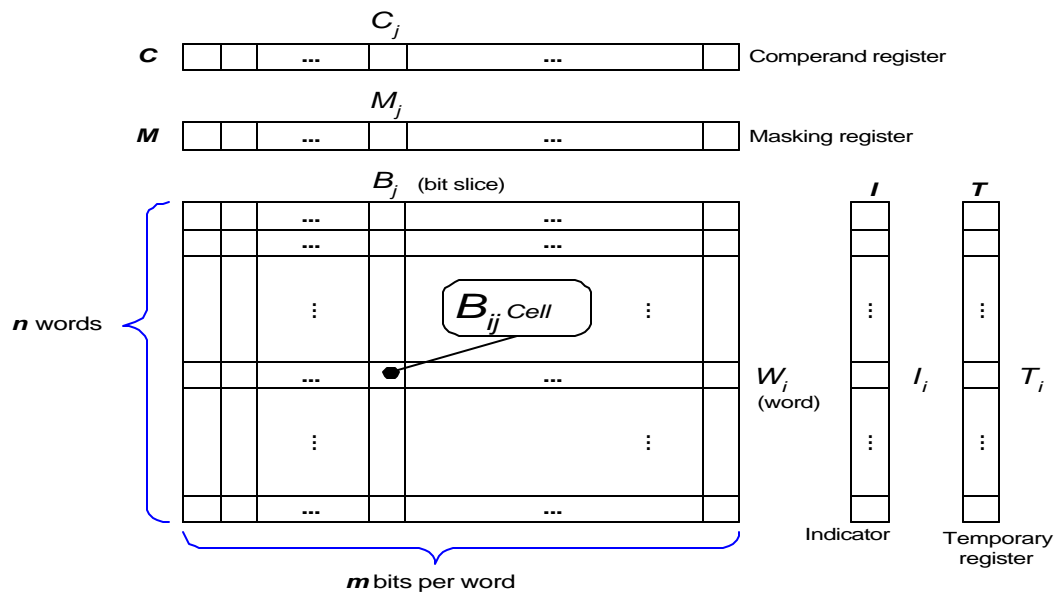
The fundamental distinction between AM and RAM is that:

- AM is **content addressable**, which allows parallel access of multiple memory words. Thus AM usually implemented together with a special class of SIMD (Single Instruction stream – Multiple Data stream) array processors, called the “associative processors architecture”. [Review Chapter 1.3 & SISD, SIMD, MISD, MIMD materials on Chapter 1.4]
- The conventional RAM has to be access sequentially by specifying the word addresses.

ASSOCIATIVE MEMORY ORGANIZATION

Data stored in AM are addressed by their contents, thus it is known as **content-addressable memory**, AM are also known as other names, **parallel search memory**, or **multi-access memory**.

The basic structure of AM is as shown.



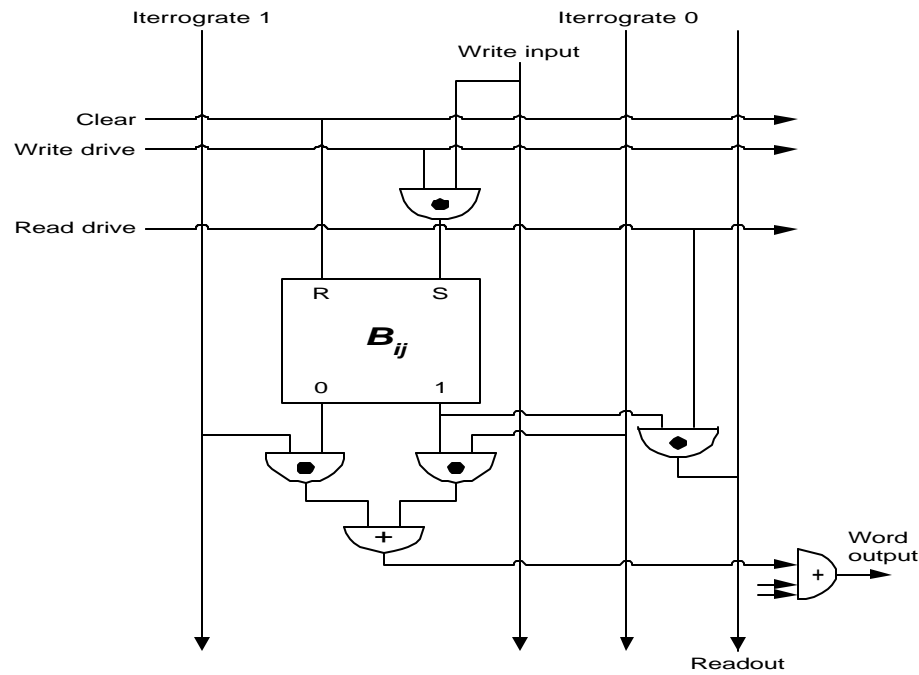
The AM memory array consist of  $n$  words with  $m$  bits each. Each bit cell in the  $n \times m$  array is a flip-flop with some comparison logic gates for pattern matching and read-write control. Thus, each bit  $B_{ij}$  cell can be individually written-in, read-out, or compared with an external signal.

A **bit slice** is a vertical column of bit cells of all the words at the same index position, denoted with  $j$  index in the picture.

The major advantage of AM compared to RAM is that it has the capability to perform **parallel search** and **parallel comparison** operations, which are frequently required in many important applications (e.g. storage and retrieval of rapidly changing databases, radar-signal tracking, image processing, computer vision and artificial intelligence). The major disadvantage of AM is that it required a more costly hardware to be properly implemented.

A parallel search operations involve both comparison and masking registers and are executed according to the organization of the associative memory. The **comparand register C** is used to hold the key operand being searched for or being compared with. The **masking register M** is used to enable or disable the bit slices to be involved in the parallel comparison operations across all the words in the AM. The **indicator register I** and one or more **temporary registers T** are used to hold the current and previous match patterns. Each of these registers can be set, reset or loaded from an external source with any desired binary patterns. The **counters** are used to keep track of the  $i$  and  $j$  index values.

The search key in the C register is first masked by the bit pattern in the M registers, this masking operation selects the effective fields of bit slices to be involved. Parallel comparisons of the masked key word with all words in the associative memory are performed by sending the proper interrogating signals to all the bit slices involved. All of the involved bit slices are compared in parallel or in sequential order, depending on the AM organization. If multiple word in the AM match the search pattern, the indicator register is required to tag all the matched words and temporary registers hold the matched word values.



Interrogation Information	Mask	Information Stored	
		0	1
0	0	0	0
1	0	0	0
0	1	0	1
1	1	1	0

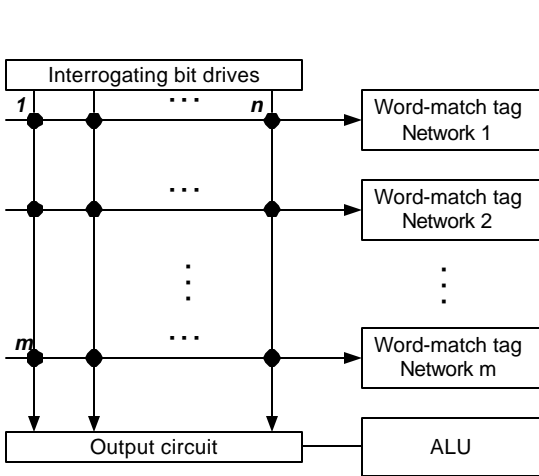
**Mask bit** value of 0 indicating that there is no comparison performed at that particular bit position (index) of all words.

There are 2 types of comparison readout in AM, the **bit-cell readout** and the **word readout**. The two are needed in two different AM organizations.

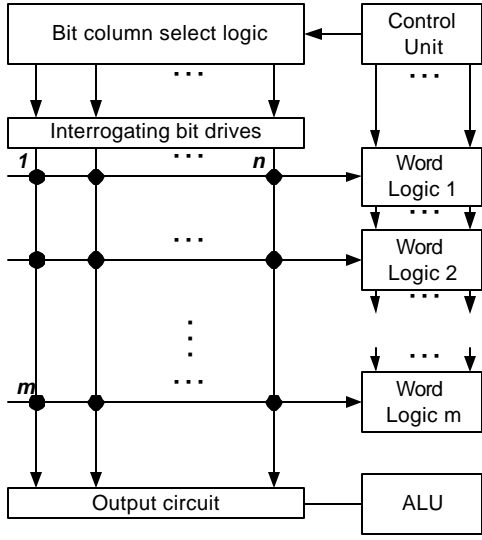
Most AM have the capability of **word parallel operation**, which is all word in the AM array are involved in the parallel search operations. This operation is differ greatly with RAM's **word serial operations**.

Based on how bit slices are involved in the operations, there are 2 different AM organization possible.

- The **bit parallel organization**, is an AM organization where the comparison process is performed in a parallel-by-word and parallel-by-bit fashion. All bit slices which are not masked off by the masking pattern are involved in the comparison process. In this organization, word-match tags for all of the word are used.
- and **bit serial organization**, is an AM organization which operates with one bit slice at a time across all of the words. The particular bit slice is selected by an extra logic and control unit. The bit-cell readouts will be used in subsequent bit-slice operations.



**bit parallel organization**



**bit serial organization**

The AM memories are used mainly for search and retrieval of non-numeric information. The bit serial organization requires less hardware but is slower in speed. The bit parallel organization requires additional word-match detection logic but is faster in speed.